

ABSTRACT OF THE DISCLOSURE

A split gate, vertical NROM memory cell is comprised of a plurality of oxide pillars that each has a source/drain region formed in the top of the pillar. A trench is formed between each pair of oxide pillars. A polysilicon control gate is formed in the trench between the pair of oxide pillars. A polysilicon program gate is formed between the control gate and each oxide pillar. The program gates extend along the sidewall of each oxide pillar. A gate insulator layer is formed between each program gate and the adjacent oxide pillar. Each gate insulator layer has a structure for trapping at least one charge. In one embodiment, the gate insulator structure is an oxide-nitride-oxide layer in which the charge is stored at the trench bottom end of the nitride layer. An interpoly insulator is formed between the program gates and the control gate.